

What Is Claimed Is:

1 1. An apparatus for detecting errors on a source-synchronous bus,
2 comprising:
3 the source-synchronous bus, wherein the source-synchronous bus includes
4 a plurality of data lines and a clock line;
5 a transmitting mechanism coupled to the source-synchronous bus, wherein
6 the transmitting mechanism is configured to transmit data on the source-
7 synchronous bus;
8 a receiving mechanism coupled to the source-synchronous bus, wherein
9 the receiving mechanism is configured to receive data from the source-
10 synchronous bus; and
11 an error detecting mechanism coupled to the receiving mechanism that is
12 configured to detect errors on the source-synchronous bus;
13 wherein the error detecting mechanism can detect errors on the plurality of
14 data lines including errors that are caused by an error on the clock line.

1 2. The apparatus of claim 1, wherein the apparatus further comprises:
2 a grouping mechanism coupled to the transmitting mechanism that is
3 configured to group data bits into an error group;
4 a detection code generating mechanism coupled to the grouping
5 mechanism that is configured to generate a detection code for the error group; and
6 the transmitting mechanism that is further configured to transmit the
7 detection code on the source-synchronous bus using a clock cycle other than the
8 clock cycles used for transmitting data bits of the error group.

1 3. The apparatus of claim 2, wherein the detection code is a parity bit.

1 4. The apparatus of claim 2, wherein the detection code is an error
2 correcting code.

1 5. The apparatus of claim 2, wherein the grouping mechanism is
2 further configured to skew data bits within the error group across time.

1 6. The apparatus of claim 5, wherein skewing data bits across time
2 includes delaying a data bit based on a position of the data bit within the error
3 group.

1 7. The apparatus of claim 5, further comprising a gathering
2 mechanism coupled to the receiving mechanism, wherein the gathering
3 mechanism is configured to de-skew data bits within the error group.

1 8. A method for detecting errors on a source-synchronous bus,
2 wherein the source-synchronous bus includes a plurality of data lines and a clock
3 line, the method comprising:
4 transmitting data from a source on the source-synchronous bus;
5 receiving data at a destination from the source-synchronous bus; and
6 detecting data errors at the destination, wherein detecting data errors
7 includes detecting errors that are caused by errors on the clock line.

1 9. The method of claim 8, further comprising:
2 grouping data bits into an error group;
3 generating a detection code for the error group; and

4 transmitting the detection code on the source-synchronous bus using a
5 clock cycle other than the clock cycles used for transmitting data bits of the error
6 group.

1 10. The method of claim 9, wherein the detection code is a parity bit.

1 11. The method of claim 9, wherein the detection code is an error
2 correcting code.

1 12. The method of claim 9, further comprising skewing data bits
2 within the error group across time.

1 13. The method of claim 12, wherein skewing data bits across time
2 includes delaying a data bit based on a position of the data bit within the error
3 group.

1 14. The method of claim 12, further comprising de-skewing data bits
2 within the error group.

1 15. A computing system for detecting errors on a source-synchronous
2 bus, comprising:
3 the source-synchronous bus, wherein the source-synchronous bus includes
4 a plurality of data lines and a clock line;
5 a central processing unit coupled to the source-synchronous bus, wherein
6 the central processing unit is configured to transmit data on the source-
7 synchronous bus;

8 a memory unit coupled to the source-synchronous bus, wherein the
9 memory unit is configured to receive data from the source-synchronous bus; and
10 an error detecting mechanism coupled to the memory unit that is
11 configured to detect errors on the source-synchronous bus;
12 wherein the error detecting mechanism can detect errors on the plurality of
13 data lines including errors that are caused by an error on the clock line.

1 16. The computing system of claim 15, wherein the computing system
2 further comprises:

3 a grouping mechanism coupled to the central processing unit that is
4 configured to group data bits into an error group;
5 a detection code generating mechanism coupled to the grouping
6 mechanism that is configured to generate a detection code for the error group; and
7 the central processing unit that is further configured to transmit the
8 detection code on the source-synchronous bus using a clock cycle other than the
9 clock cycle used for the error group.

1 17. The computing system of claim 16, wherein the detection code is a
2 parity bit.

1 18. The computing system of claim 16, wherein the detection code is
2 an error correcting code.

1 19. The computing system of claim 16, wherein the grouping
2 mechanism is further configured to skew data bits within the error group across
3 time.

1 20. The computing system of claim 19, wherein skewing data bits
2 across time includes delaying a data bit based on a position of the data bit within
3 the error group.

1 21. The computing system of claim 19, further comprising a gathering
2 mechanism coupled to the memory unit, wherein the gathering mechanism is
3 configured to de-skew data bits within the error group.